AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1 - 6 (canceled).

7. (currently amended): A clock control circuit comprising:

a stage to which a plurality of clocks of mutually different phases are input, this stage generating a plurality of control signals based on the ~~corresponding to~~ transition timing of one clock of the plurality of clocks and on ~~to~~ phase differences between the plurality of clocks;

a switch group, whose switching is controlled by the control signals, for controlling charging and discharging of a capacitor, wherein the phase differences between the clocks vary the charging or discharging speed of the capacitor by shifting the switch control timings of switches in the switch group; and

a stage of converting terminal voltage of the capacitor to a logic signal and outputting the logic signal.